What is claimed

1. A method for verifying a generated computer code having a plurality of lines generated from a model of a system comprising:

processing the model to determine an expected computer code having a plurality of lines based on the model; and

comparing the generated computer code to the expected computer code to determine if the generated computer code includes all of the lines of the expected computer code.

2. The method of claim 1 further comprising the step of comparing each of the lines of the generated computer code to an expected form to verify each of the lines of the generated computer code is in a proper format.

3. The method of claim 1 further comprising the step of comparing the generated computer code to the expected computer code to determine if the generated computer code includes any line of code not in the expected computer code.

4. The method of claim 1 further comprising the step of comparing the generated computer code to the expected computer code to determine if the lines of the generated computer code are in a logical order.

5. The method of claim 1 further comprising the step of comparing a header information section of the generated computer code to an expected header information section to determine if the header information section of the generated computer code matches the expected header information.

6. The method of claim 1 further comprises comparing a generated declared variable section of the generated computer code to an expected declared variable section of an expected computer code to determine if the generated declared variables section matches the expected declared variable section.

7. A computer-readable storage medium containing a set of instructions for verifying a generated computer code having a plurality of lines, the generated computer code automatically generated from a model of a system, the set of instructions comprising:

code that reads in a model file;

code that determines an expected computer code having a plurality of lines based on the model file;

code that reads in the generated computer code; and

code that compares the generated computer code to the expected computer code to determine if the generated computer code includes all the lines of the expected computer code.

8. The medium of claim 7 wherein the set of instructions further comprises code that compares each of the lines of the generated computer code to an expected form.

9. The medium of claim 7 wherein the set of instructions further comprises code that compares the generated computer code to the expected computer code to determine if the generated computer code includes any line of code not in the expected computer code.

10. The medium of claim 7 wherein the set of instructions further comprises code that compares the generated computer code to the expected computer code to determine if the lines of the generated computer code are in a logical order.

11. The medium of claim 7 wherein the set of instructions further comprises code that compares a header information section of the generated computer code to an expected header information section to determine if the header information section of the generated computer code matches the expected header information.

12. A system for verifying the contents of a generated computer code generated from a model comprising:

a processor operable to compare the generated computer code with an expected computer code, the expected computer code determined by the processor from the model; and

a display coupled to the processor, the display displaying a result of the comparisons.

13. The system of claim 12 wherein the results of the comparison indicates if the generated computer code has all of the content of the expected computer code.

14. The system of claim 12 wherein the results of the comparison indicates if the generated computer code has any additional content not found in the expected computer code.

15. The system of claim 12 wherein the processor means is operable to compare each of the lines of code in the generated computer code to an expected form.

16. The system of claim 12 wherein the processor means is operable to compare the generated computer code to the expected computer code to determine if the generated computer code includes any line of code not in the expected computer code.

17. The system of claim 12 wherein the processor means is operable to compare the generated computer code to the expected computer code to determine if the lines of the generated computer code are in a logical order.

18. The system of claim 12 wherein the processor means is operable to compare a header information section of the generated computer code to an expected header information section stored in a database or stored via other means to determine if the header information section of the generated computer code matches the expected header information.

19. The system of claim 12 wherein the model is a model of an aircraft control system.

20. The system of claim 12 wherein the result of the comparison satisfies DO-178B.